## REMARKS/ARGUMENTS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 1-20 are pending in this case. .

The outstanding Official Action includes a rejection of Claims 1-3, 6-8, 11-13, and 16-20 under 35 U.S.C. §103(a) as being unpatentable over Kan (U.S. Patent No. 5,355,508) in view of Venable (U.S. Patent No. 6,705,456), a rejection of Claims 4, 9, and 14 under 35 U.S.C. §103(a) as unpatentable over Kan in view of Venable in further view of Arimilli et al. (U.S. Patent No. 6,023, 746, Arimilli), a rejection of Claims 5, 10, and 15 under 35 U.S.C. §103(a) as unpatentable over Kan in view of Venable in further view of Yamagami et al. (U.S. Patent No. 6,229,954, Yamagami).

The rejection of Claims 1-3, 6, 7, 11, 12, and 16-20 under 35 U.S.C. §103(a) as being unpatentable over <u>Kan</u> in view of <u>Venable</u> is again traversed.

The first full paragraph under the statement of this rejection (item 7 on page 6 of the outstanding Action) relies upon Kan as teaching "an arithmetic processing unit" as to elements 108 shown in Figure 2 with apparent reference to the recital in independent Claim 1 of "an arithmetic processing unit configured to process image data relating to the image data received by the sensor board unit to provide processed image data representing a reproduction of said original document." This paragraph then incorrectly states that Claim 1 as recites "said processing unit including." In Actuality, Claim 1 recites "said arithmetic processing unit including" (emphasis added). The recitation that it is "said arithmetic processing unit" that must include the further recited elements of "a programmable arithmetic processing section," a memory," "a control register section," and "a memory controller section" cannot be ignored because it is well established that each word of each claim must be given weight. See In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Thus, if the requirement actually stated by Claim 1 is considered, as it must be, then the PTO must demonstrate how <u>Kan</u> in view of <u>Venable</u> teach the requirement of Claim 1 that the "<u>arithmetic</u> processing unit" (emphasis added), and not some other "processing unit," includes the above noted Claim 1 elements.

In this respect, the fact that <u>Kan</u> teaches the "arithmetic processing unit" 108 to be included in the "programmable arithmetic processing section of SIMD" cannot be said to teach the opposite arrangement of these elements, which is what Claim 1 requires.

Just as the SIMD programmable arithmetic processing section of <u>Kan</u> cannot be reasonably said to be included in element 108, neither can the Claim 1 "memory configured with a plurality of addressable memory locations." This is also true as to the Claim 1 recited "control register section configured to receive control inputs directly from a control unit," and the Claim 1 "memory controller section," both of which are clearly outside element 108, not a part included in element 108.

Thus, the outstanding Action is in error in suggesting that the Claim 1 recited "memory" can be read on elements 42 and 98-101 of Figure 2 of <u>Kan</u>, that the Claim 1 recited "control register section" can be read on element 11of Figure 2 of <u>Kan</u>, and that the Claim 1 recited "memory controller section" can be read on element 103 of Figure 2 of <u>Kan</u>. All of these Figure 2 elements (42 and 98-101, 11, and 103) are clearly disclosed to be separate from elements 108, not included as a constituent part of element 108.

Independent Claim 6 recites similar limitations to those in independent Claim 1, but in "means-plus function form. Thus, Claim 6, *inter alia*, requires:

means for performing processing of image data relating to the image data received by the sensor board means to provide processed image data representing a reproduction of said original document, said arithmetic processing means including,

a programmable arithmetic processing means of SIMD (Single Instruction Multiple Data stream) type for performing simultaneous processing of plural a- image data portions,

memory means having a plurality of addressable memory locations, with each memory location storing image data portions relating to the image data received by the sensor board means,

a control register means for receiving control inputs directly from a separate control means, said separate control means being external to said arithmetic processing means, said control register means further processing said control inputs to provide control register means outputs, and

a memory controller means for controlling access to at least some of said addressable memory locations in response to the control register means outputs to control transfer of the image data portions stored thereat to said programmable arithmetic processing section means as said plural image data portions undergoing said simultaneous processing to provide said processed image data representing the reproduction of said original document.

Just as the rejection of independent Claim 1 was clearly based upon improperly interpreting the required arrangement of elements recited by independent Claim 1, the rejection of independent Claim 6 is clearly based upon improperly interpreting the similar arrangement of the means required by independent Claim 6.

Furthermore, the case law is clear as to the broadest reasonable interpretation that can be applied to any "means" claim being the interpretation statutorily mandated by the sixth paragraph of 35 U.S.C.§112. *See in re Donaldson Co.*, 16 F.3d 1189, 1194-95, 29 USPQ2d 1845, 1850 (Fed. Cir.1994) (in banc). Clearly missing here is any explanation of how controllers 103 and 11, of unknown makeup, are being interpreted to be equivalent to the disclosed "control register means" and the "memory controller means," for example.

Moreover, the method steps of independent method Claim 11 and the similar steps associated with the computer readable medium of Claim 16 have not been properly analyzed and explained in terms of how <u>Kan</u> in view of <u>Venable</u> can be reasonably said to teach the recited method steps including:

receiving data representing said scanned document image from a sensor board unit;

receiving control inputs directly from a control unit at a control register section, said control unit being external to said arithmetic processing section; processing said control inputs at said control register section to provide control register section outputs to the memory controller section;

controlling transfer of at least some of the image data portions related to the scanned document image between said addressable memory locations and said arithmetic processing section by using said memory controller section under control of said control register section outputs and controlling transfer of processed data from said programmable arithmetic processing section to provide a processed reproduction of said scanned document image; and

transferring the processed reproduction of said scanned document image to a second document.

Claim 2 and Claims 17-20 are dependent from independent Claim 1, Thus, Claims 2 and 17-20 are also believed to be patentable for the reasons noted above as to parent Claim 1 as well as for the reason that the added subject matter thereof is not taught or suggested by Kan and/or Venable taken alone or together in any proper combination.

As Claims 7 and 8 depend on Claim 6 and as Claims 12 and 13 depend on Claim 11, these dependent claims are believed to patentably define over <u>Kan</u> in view of <u>Venableer</u> for reasons noted above as to respective parent Claims 6 and 11. In addition, the rejection of dependent Claims 7, 8, 12, and 13 under 35 U.S.C. §103(a) as unpatentable over <u>Kan</u> in view of <u>Venable</u> is traversed because these dependent claims also recite additional features not taught or suggested by the applied references.

Applicants respectfully traverse the rejection Claims 4, 9, and 14 under 35 U.S.C. §103(a) as unpatentable over <u>Kan</u> in view of <u>Venable</u> in further view of <u>Arimilli</u> and the rejection of Claims 5, 10, and 15 under 35 U.S.C. §103(a) as unpatentable over <u>Kan</u> in view of <u>Venable</u> in further view of <u>Yamagami</u>. In this regard, neither <u>Arimilli</u> nor <u>Yamagami</u> cures the above noted deficiencies of the primary combination of Kan and Venable.

Applicants further respectfully traverse the rejection of Claims 4, 9, and 14 under 35 U.S.C. §103(a) as unpatentable over <u>Kan</u> in view of <u>Venable</u> in further view of <u>Arimilli</u> and the rejection of Claims 5, 10 and 15 under 35 U.S.C. §103(a) as unpatentable over <u>Harrell</u> in

Application No. 09/749,819 Reply to Office Action of 11/07/05

view of <u>Venable</u> and further in view of <u>Yamagami</u> because Claims 4, 5, 9, 10, 14, and 15 recite additional features not taught or suggested by the applied references.

Accordingly, the outstanding rejections are traversed and the pending claims are believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,

MAIER & NEUSTADT, PAC.

Customer Number 22850

Tel: (703) 413-3000 Fax: (703) 413 -2220 (OSMMN 06/04)

I:\ATTY\RFC\20\201392.REQFORRECON.DOC

Gregory J Maier Attorney of Record Registration No. 25,599

Raymond F. Cardillo, Jr. Registration No. 40,440